UNITED STATES PATENT APPLICATION

OF

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FOR

DIGITAL TV RECEIVER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001]   This application claims the benefit of Korean Application No. P2002-74220, filed

on November 27, 2001, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002]   The present invention relates to a digital TV receiver, and more particularly, to an

apparatus for recovering a symbol clock from received data.

Discussion of the Related Art

[0003]   An advanced television systems committee (ATSC) 8 VSB (Vestigial Side Band)

transmission system proposed by most current digital transmission systems and a US directed

digital TV transmission mode loads data only in a transmission signal to increase an effect of a

frequency. That is, clock information needed for data recovery at a receiving party is not

transmitted. Therefore, the same clock as that employed during the transmission should be

generated among the received signals having only data to recover the data at the receiving party. A symbol clock recovery performs the role.

[0004] FIG. 1 is a block diagram illustrating a general digital TV receiver having such symbol clock recovery. Referring to FIG. 1, if a radio frequency (RF) signal modulated in a VSB mode is received through an antenna 101, a tuner 102 selects a desired channel frequency. Then, the tuner 102 converts a VSB signal of an RF band inserted in the channel frequency to a first intermediate frequency (IF) band, and outputs to an analog processor 103. The analog processor 103 performs passband filtering and gain controlling to the first IF signal outputted from the tuner 102 for converting the first IF signal into a second IF signal, and outputs to an A/D converter 104. The A/D converter 104 samples the second IF signal with a fixed frequency (i.e., the fixed frequency is different from the symbol clock frequency, and normally 25MHz), and outputs to a phase splitter 105. That is, the data sampled at 21. 52MHz two times the frequency of the symbol clock is received at the receiving party although the outputted data from the A/D converter 104 is digital data sampled at 25MHz.

[0005] The phase splitter 105 splits the digital signal into a passband real signal r(t)) and a passband imaginary signal (i(t)), and outputs the signal to the carrier recovery 106. At this time, for easier description, the real/imaginary signals outputted from the phase splitter 105 is named as I and Q signals, respectively.

[0006] The carrier recovery 106 converts the digital signals I and Q of the passband outputted from the phase splitter 105 to a baseband. The output signal of the carrier recovery 106 is inputted to a symbol clock recovery 107, a synchronized signal detector 108 and a digital processor 109.

[0007] At this time, the symbol clock recovery 107 recovers all the symbol clocks employed by from the carrier recovery 106 to the digital processor 109 and the synchronized signal detector 108 detects a segment sync and a field sync from the digital baseband signal.

[0008] FIG. 2 is a block diagram of the carrier recovery 106 employing a FPLL (Frequency Phase Locked Loop). That is, the carrier recovery 1068 having the FPLL demodulates the passband I and Q signals outputted from the A/D converter 1045 into the baseband I and Q signals for frequency and phase locking.

[0009] Referring to FIG.2, the passband I and Q signals being digitized through the A/D converter 104 and the phase splitter 105 are inputted to a complex multiplier 201 of the carrier recovery. At this time, the real signal (r(t)) and the imaginary signal (q(t)) outputted from the phase splitter 105 is expressed as a following formula.

[0010] [Formula 1]

$$r(t)=\{I(t)+p\}\cos(w_c t + \Psi) - Q(t)\sin(w_c t + \Psi)$$

$$i(t)=\{I(t)+p\}\sin(w_c t + \Psi) + Q(t)\cos(w_c t + \Psi)$$

4

[0011] I(t) is a signal before a modulation and p is a pilot signal inputted to the transmitter for the carrier recovery. Also, w_c is thea frequency of the carrier signal existing in an input signal and Ψ psi is a phase of the carrier signal existing in the input signal. Q(t) is an an orthogonal signal component of I(t).

[0012] Meanwhile, the complex multiplier 201 of the carrier recovery 106 multiplies the passband I and Q signals as the formula 1 by a standard carrier signals NCOI and NCOQ outputted from the NCO 205, and converts the passband I and Q signal into the baseband I and Q signals (I'(t),Q'(t)) as a following formula 2.

[0013] [Formula 2]

$$I'(t)=\{I(t)+p\}\cos(\Delta w_c t+\Psi)-Q(t)\sin(\Delta w_c t+\Psi)$$

$$Q'(t)=\{I(t)+p\}\sin(\Delta w_c t+\Psi)+Q(t)\cos(\Delta w_c t+\Psi)$$

[0014] The Δw_c is a beat frequency of the carrier signal w_c employed by the transmitter and the standard carrier signals NCOI and NCOQ generated from the receiver.

[0015] The I and Q signals of the baseband are outputted to a low pass filter 202 as well as to the symbol clock recovery 1087 and the digital processor 109 through the resampler 107.

[0016] The low-pass filter 202 filters the low pass I and Q signals to extract the carrier and outputs to an error detector 203. That is, the carrier recovery 106 recovering the carrier needs only signals around the frequency having the pilot frequency in a band width of 6MHz and,

5

therefore, the low-pass filter prevents the efficiency of the carrier recovery from being reduced

by removing the remaining frequency component having data component from the I and Q

signals.

[0017]   The error detector 203 detects remaining error of the carrier from the carrier

signal, and outputs to the low-pass filter 204. That is, the remaining carrier error detected from

the error detector 203 is outputted to an NCO 205 through the low-pass filter 204 to prevent

errors from being accidentally detected. The NCO 205 generates new carrier signals NCOI and

NCOQ and outputs to the complex multiplier 201.

[0018]   If the carrier recovery is completely performed at the carrier recovery 106, $\Delta w_c t$

and Ψ become '0', and the formula 2 will be changed to a following formula 3.

[0019]   [Formula 3]

$I'(t)=I(t)+p$

$Q'(t)=Q(t)$

[0020]   The symbol clock recovery 10_78 performs the symbol clock recovery from the

signal of the formula 3 and generates the symbol clocks employed in all digital areas of the

receiver.

[0021]   However, if the carrier recovery is not completely carried out in the carrier

recovery 106, the symbol clock recovery 10_78 recovers the symbol clock from the signal of the

6

formula 2. Thus, the symbol clock recovery is not normally performed being influenced by the frequency and the phase between the carrier signals employed by the receiver and the standard carrier signal generated from the receiver such as Δw_c and Ψ.

[0022]   In other words, as described in FIG. 1, the performance of the carrier recovery largely influences the performance of the symbol clock recovery in a structure the carrier recovery and the symbol clock recovery is connected. The symbol clock recovery is influenced by the remaining frequency and phase error not completely removed from the carrier recovery, and that gives bad influence on the total performance of the symbol clock recovery.

[0023]   The reason why the symbol clock recovery is located at an end of the general carrier recovery is that the symbol clock recovery is designed under an assumption that the role of the carrier recovery is completed. Therefore, if the carrier recovery is not completely performed, the symbol clock recovery is not performed as well.

SUMMARY OF THE INVENTION

[0024]   Accordingly, the present invention is directed to a digital TV receiver for recovering a symbol clock irrespective of the remaining phase and phase error of the carrier recovery that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0025] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0026] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the digital TV receiver includes an A/D converter for converting an analog passband signal into a digital passband signal, a carrier recovery for converting the digital passband signal into a digital baseband signal, a symbol clock recovery for generating and outputting the two times frequency of the symbol clock corrected from the detected timing error information.

[0027] In another aspect of the present invention, the digital TV receiver includes the A/D converter for sampling the analog passband signal with a fixed frequency generated from the fixed oscillator and converting the digital passband signal, the carrier recovery for multiplying the digital passband signal by a standard carrier signal generated from the carrier recovery to convert the digital passband signal into the digital baseband signal, a first resampler for resampling the digital baseband real/imaginary signals generated from the carrier recovery to

two times frequency and interpolating each of them, the symbol clock recovery for detecting

timing error information from the digital passband signal or the digital baseband signal and

generating and outputting the two times frequency recovered from the detected timing error

information.

[0028]   In this case, the symbol clock recovery includes an operator for calculating each

of the digital baseband real/imaginary signals interpolated and outputted from the first resampler,

and outputting the calculation; a pre-filter for passing only a frequency of a particular band to

recover the symbol clock from the output of the operator; a timing error detector for detecting

timing error information from the output of the pre-filter; a filtering unit for filtering only a low

passband signal from the timing error information outputted from the timing error detector; and a

NCO for generating two times the frequency of the symbol clock recovered according to low

pass signal component of the filtered timing error information and outputting to the first

resampler.

[0029]   The operator squares each of the digital baseband real/imaginary signals

interpolated and outputted from the first resampler, adds the two squared signals, and outputs the

calculation; or calculate an absolute value for each of the digital baseband real/imaginary signals

interpolated and outputted from the first resampler, adds the absolute value of the two signals,

and outputs the calculation.

[0030]   The symbol clock recovery includes a second resampler for resampling the digital passband real/imaginary signals outputted from the A/D converter into the two times the frequency of the symbol clock and interpolating each of the signals; a operator for calculating the digital passband real/imaginary signals outputted from the second resampler and outputting the calculation; a pre-filter for passing only a frequency of a particular band to recover the symbol clock fromthe output of the operator; a timing error detector for detecting timing error information from the output of the pre-filter; a NCO for generating two times the frequency of the symbol clock recovered according to low pass signal component of the filtered timing error information and outputting to the first resampler and the second resampler.

[0031]   In this case, the operator squares each of the digital baseband real/imaginary signals interpolated and outputted from the second resampler, adds the two squared signals, and outputs the calculation; or calculate an absolute value for each of the digital baseband real/imaginary signals interpolated and outputted from the second resampler, adds the absolute value of the two signals, and outputs the calculation.

[0032]   The symbol clock recovery includes an A/D converter for taking a sample of a fixed frequency from an analog passband signal and converting into a digital passband signal; a carrier recovery for multiplying a standard carrier signal generated from the process of the carrier recovery of the digital passband signal and converting into the digital baseband signal; and a

10

symbol clock recovery for detecting timing error information from the digital passband signal or the digital baseband signal and generating and outputting the two times the frequency of the symbol clock corrected from the detected timing error information.

[0033]   The symbol clock recovery includes a operator for calculating each of the digital baseband real/imaginary signals outputted from the carrier recovery, and outputting the calculation; a pre-filter for passing only a frequency of a particular band to recover the symbol clock from the output of the operator; a timing error detector for detecting timing error information from the output of the pre-filter; a filtering unit for filtering only the low passband signal from the timing error information outputted from the timing error detector; and a variable oscillator for generating two times the frequency of the symbol clock recovered according to low pass signal component of the filtered timing error information and outputting to the A/D converter.

[0034]   In this case, the operator squares each of the digital baseband real/imaginary signals interpolated and outputted from the carrier recovery, adds the two squared signals, and outputs the calculation; or calculate an absolute value for each of the digital baseband real/imaginary signals interpolated and outputted from the carrier recovery, adds the absolute value of the two signals, and outputs the calculation.

11

[0035]   Also, the symbol clock recovery includes a operator for calculating each of the

digital baseband real/imaginary signals interpolated and outputted from the first resampler, and

outputting the calculation; a pre-filter for passing only a frequency of a particular band to recover

the symbol clock fromthe output of the operator; a timing error detector for detecting timing

error information from the output of the pre-filter; a filtering unit for filtering only the low

passband signal from the timing error information outputted from the timing error detector; and a

variable oscillator for generating two times the frequency of the symbol clock recovered

according to low pass signal component of the filtered timing error information, and outputting

to the A/D converter.

[0036]   In this case, the operator squares each of the digital baseband real/imaginary

signals outputted from the A/D converter, adds the two squared signals, and outputs the

calculation; or calculate an absolute value for each of the digital baseband real/imaginary signals

outputted from the A/D converter, adds the absolute value of the two signals, and outputs the

calculation.

[0037]   It is to be understood that both the foregoing general description and the

following detailed description of the present invention are exemplary and explanatory and are

intended to provide further explanation of the invention as claimed.

12

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings;

[0039] FIG. 1 illustrates a block diagram of a conventional digital TV receiver.

[0040] FIG. 2 is a block diagram illustrating a conventional carrier recovery of FIG. 1.

[0041] FIG. 3 is a block diagram illustrating a digital TV receiver having a symbol clock recovery according to a first embodiment of the present invention.

[0042] FIG. 4 is a block diagram illustrating a digital TV receiver having a symbol clock recovery according to a second embodiment of the present invention.

[0043] FIG. 5 is a block diagram illustrating a digital TV receiver having a symbol clock recovery according to a third embodiment of the present invention.

[0044] FIG. 6 is a block diagram illustrating a digital TV receiver having a symbol clock recovery according to a fourth embodiment of the present invention.

[0045] FIG. 7 is a block diagram illustrating a digital TV receiver having a symbol clock recovery according to a fifth embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0046]   Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0047]   As illustrated in FIG.3, an~~the~~ A/D converter 301 takes a sample of a fixed frequency from an analog passband signal and changes to a digital passband signal. In this case, the fixed frequency oscillated in a~~the~~ fixed oscillator 302 is higher than two times the frequency of the symbol clock. Since the data rate is different and there is a difficulty in controlling, a resampler 305 needs to be arranged between a~~the~~ carrier recovery 304 and two squarers~~multipliers~~ 306 and 307 when the signal is employed in the symbol clock recovery.

[0048]   The digital passband signal outputted from the A/D~~S~~ converter 301 is inputted to the ~~the~~ carrier recovery 304 through a~~the~~ phase splitter 303~~0~~ and changed into a digital baseband signal.

[0049]   In this instance, the digital baseband signal is changed from the digital passband signal taken a sample of the fixed frequency different from the symbol clock frequency, and the digital baseband signal is taken as a sample of two times the frequency of the symbol clock at 21.52MHz, and outputted for recovering the symbol clock in the resampler 305.

14

[0050]   (I''(t)) signals of real numbers outputted from the resampler 305 are squared multiplied at thea squarermultiplier 306 and (Q''(t)) signals of imaginary numbers outputted from the resampler 305 are squared at thea squarermultiplier 307, inputted to an adder 308, and added, thereby the frequencies and phase errors resulted from an incomplete carrier recovery are removed. The output of the adder 308 is outputted to a timing error detector 310 through a pre-filter 309 passing only desired frequency bands for the symbol clock recovery and outputtted to a digital processor 313.—The timing error detector 310 is a timing error detector of a Gardner system or of a modifiedfixed Ggardner system, and detects a timing error, that is, the phase error. The timing error information is inputted to an NCO 312 through a low pass filter 311. The NCO 312 generates new corrected two times the frequency of the symbol clock (2fs, fs is a symbol clock frequency) from the timing error information and outputs to the resampler 305.

[0051]   FIG. 4 is an preferred embodiment in case that the frequency of the clock inputted to anthe A/D converter 401 is not a fixed frequency but two times frequency (2fs) although an operation and role is the same as that in FIG. 3. The output of the A/D converter is inputted to a carrier recovery 403 through a phase splitter 402. In case of FIG. 4, the A/D converter 401 takes a sample of two times the frequency of the symbol clock (2fs) from the analog passband signal and changes the signal into a digital passband signal, and, thus, the

resampler is not required between the carrier recovery 403 and the two squarersmultipliers 404

and 405. Therefore, a burden on the hardware is eased.

[0052]   Also, the output of a low-pass filter 409 for filtering the timing error information

of the current symbol detected from athe timing error detector 408 is inputted to a variablevoltage

controlled oscillator 410 generating new two times the frequency of the symbol clock (2fs), the

newly generated two times the frequency of the symbol clock (2fs) generated from the timing

error information filtered at the low pass filter 409. The output of each of the two squarers 404

and 405 are inputted to an adder 406. The output of the adder 406 is inputted to a pre-filter 407

and a digital processor 411. In this case, the roles of the squarersmultipliers 404 and 405, thethe

adder 406, the pre-filter 407309, the Gardner timing error detector 408 and the low-pass filter

409 are the same as the same block in FIG. 3.

[0053]   In this instance, input formulas {I"(t), Q"(t)} of the two squarersmultipliers in

FIG. 3 and FIG. 4 are described as a formula 3 if the carrier recovery is completely carried out

and as a formula 2 if the carrier recovery is not completely carried out. The output of the two

squarersmultipliers is the same as a following formula 4 when the carrier recovery is completed.

[0054]   [Formula 4]

$$\{I"(t)\}^2 = \{I(t)+p\}^2 = I^2(t)+p^2+2pI(t)$$

$$\{Q"(t)\}^2 = Q^2(t)$$

[0055]   If the carrier recovery is not completely carried out, the output of the two

squarersmultipliers is the same as the following formula 5.

[0056]   [Formula 5]

$$\{I''(t)\}^2 = [\{I(t)+p\}\cos(\Delta w_c t+\Psi)]^2$$

$$= \{I(t)+p\}^2\cos^2(\Delta w_c t+\Psi)]+Q^2(t)\sin^2(\Delta w_c t+\Psi)$$

$$-2\{I(t)+p\}Q(t)\cos(\Delta w_c t+\Psi)\sin(\Delta w_c t+\Psi)$$

$$\{Q''(t)\}^2 = [\{I(t)+p\}\sin(\Delta w_c t+\Psi)+Q(t)\cos(\Delta w_c t+\Psi)]^2$$

$$= \{I(t)+p\}^2\sin(\Delta w_c t+\Psi)+Q^2(t)\cos^2(\Delta w_c t+\Psi)$$

$$+2\{I(t)+p\}Q(t)\cos(\Delta w_c t+\Psi)\cos(\Delta w_c t+\Psi)$$

[0057]   The output of the adder for adding the output of two squarersmultipliers is the

same as the following formula 6 in both cases when the carrier recovery is completely carried out

and when not carried out.

[0058]   [Formula 6]

[0059] $X(t)=I^2(t)+Q^2(t)\pm p^2+2pI(t)$

[0060]   When the symbol clock recovery is carried out from the output of the adder, the

symbol clock recovery can be carried out without interference of a carrier.

[0061] Meanwhile, when the symbol clock recovery employs the two squarersmultipliers and adders for symbol clock recovery, the symbol clock recovery is able to recover the symbol clock from the passband signal not passed the carrier recovery.

[0062] Both of FIG. 5 and FIG. 6 are embodiments of above case. FIG. 5 is an embodiment showing a fixed oscillator is employed to anthe A/D converter in and athe resampler is added. FIG. 6 is an embodiment showing the resampler is removed using a variablechangeable oscillator.

[0063] First, anthe A/D converter 501 in FIG. 5 takes a sample of an analog passband signal from a fixed oscillating frequency generated from athe fixed oscillator 502 and converts into the digital passband signal. The digital passband signal is outputted to a carrier recovery 504 through a phase splitter 503 as well as outputted to a symbol clock recovery 507 for the symbol clock recovery. The carrier recovery 504 multiplies a referencestandard carrier signal completed the carrier recovery by the digital passband I, Q signals outputted through thea phase splitter 503, transmits the passband I, Q signals to the baseband I, Q signals, and outputs to a resampler 505 to convert into a symbol recovered signal. The resampler 505 performs sampling of I, Q signals to two times the frequency of the symbol clock (2fs) outputted from the symbol clock recovery 507 and outputs to a digital processor 506.

[0064]   Meanwhile, the symbol clock recovery 507 includes a resampler 507a for sampling the digital passband I, Q signals outputted from the phase splitter 503 for two times the frequency of the symbol clock (2fs), a squarer 507b for squaring a digital passband real number signal (I"(t)) outputted from the resampler 507a, a squarer 507c for squaring the imaginary number signal (Q"(t)), an adder 507d for adding the two squared values outputted from the two squarersmultipliers 507b and 507c, a pre-filter 507e for passing only an edge part of the output spectrum of the adder 507d, a timing error detector 507f for detecting information relating to timing error from the signals passed through the pre-filter 507e, a low pass filter 507g for filtering only low pass signal component from the timing error information outputted from the timing error detector 507f and an NCO 507i for newly generating two times the frequency of the symbol clock (2fs) according to low pass component of the timing error information, and controlling sampling timing of the resamplers 507a and 505.

[0065]   The resampler 507a of the symbol clock recovery 507 composed as such takes a sample of two times the frequency of the symbol clock (2fs) generated from the NCO 507i from the digital passband I, Q signals outputted from the phase splitter 503 and outputs the interpolated digital passband I, Q signals to each of the squarers 507b and 507c. Each of the two squarers 507b and 507c are nonlinear, respectively squares the passband I, Q signals, and outputs

the signals to the adder 507d. When the two squared signals are added at the adder 507d, the signal is changed into the baseband I, Q signals from which the carrier is removed.

[0066]The output of the adder 507d passes through the pre-filter 507e, the Gardner timing error detector 507f, the low pass filter 507g, the NCO 507i and generates new two times the frequency of the symbol clock (2fs). The resamplers 505 and 507a outputs recovered signals usinggn the two times the frequency of the symbol clock (2fs).

[0067][0066]   In this instance, a formula 7 describing the passband I, Q signals (I'''(t), Q'''(t)) inputted to the two squarers 507b and 507c is as follows.

[0068][0067]   [Formula 7]

$$I'''(t)=\{I(t)+P\}\cos(w_c t +\Psi)-Q(t)\sin(w_c t +\Psi)$$

$$Q'''(t)=\{I(t)+p\}\sin(w_c t +\Psi)+Q(t)\cos(w_c t +\Psi)$$

[0069][0068]   The formula 7 shows that signals inputted to the squarers 507b and 507c are not passing through the carrier recovery 504, and the carrier remains therein.

[0070][0069]   If the passband I, Q signals (I'''(t), Q'''(t)) the carrier remains the same therein pass through each of the squarers 507b and 507c, the formula is shown as Formula 8.

[0071][0070]   [Formula 8]

$$\{I'''(t)\}^2 = [\{I(t)+p\}\cos(w_c t +\Psi)-Q(t)\sin(w_c t +\Psi)]^2$$

$$= \{I(t)+p\}^2\cos^2(w_c t +\Psi)+Q^2(t)\sin^2(w_c t +\Psi)$$

20

$$-2\{I(t)+p\}Q(t)\cos(w_c t + \Psi)\sin(w_c t + \Psi)$$

$$\{Q'''(t)\}^2 = [\{I(t)+p\}\sin(w_c t + \Psi)+Q(t)\cos(w_c t + \Psi)]^2$$

$$=\{I(t)+p\}^2\sin^2(w_c t + \Psi)+ Q^2(t)\cos^2(w_c t + \Psi)$$

$$+2\{I(t)+p\}Q(t)\sin(w_c t + \Psi)\cos(w_c t + \Psi)$$

[0072][0071]   The formula 8 shows that the carrier remains the same. However, the carrier

signal component is removed as in Formula 9 if the output of each of the two squarers 507b and

507c such as the formula 8 is added to the adder 507d.

[0073][0072]   [Formula 9]

[0074][0073] $X'(t) = I^2(t)\pm = Q^2(t)\pm = p^2\pm = 2pI(t)$

[0075][0074]   Therefore, there is an advantage of using the symbol clock recovery that the

symbol clock is recovered from the passband signals without being interfered by the carrier.

[0076][0075]   In other words, there is an advantage that the symbol clock is recovered in a

precise and stable way without passing through the carrier recovery, that used to be a mandatory

process for the symbol clock recovery in the embodiment of FIG. 5. This describes that the

symbol clock recovery 507 is able to operate and perform more stable symbol clock recovery

regardless of the carrier signal component.

[0077][0076]   FIG. 6 describes anthe A/D converter 601 taking a sample of the analog passband signal from the two times the frequency of the symbol clock (2fs) generated from the variable oscillator instead of the fixed oscillator of FIG. 5, and converting into the digital passband signal.

[0078][0077]   aThe symbol clock recovery 605 performs the symbol clock recovery using the passband I, Q signals outputted from athe phase splitter 602 as well. The output of the carrier recovery 603 is inputted to a digital processor 604.

[0079][0078]   In FIG. 6, the A/D converter 601 performs sampling by receiving the two times the frequency of the symbol clock (2fs), and the resampler is not required.

[0079]   The symbol clock recovery 605 includes a squarer 605a for squaring the digital passband real number signal (I'''(t)) split and outputted from the phase splitter 602, a squarer 605b for squaring the digital passband -imaginary signal (Q'''(t)), an adder 605c for adding the two squared values outputted from the two squarers 605a and 605b, a pre-filter 605d for passing only the edge portion of the output spectrum of the adder 605d, a timing error detector 605e for detecting information relating to timing error from the signals passed through the pre-filter 605d, a low pass filter 605f for filtering the low pass signal components from the timing error information outputted from the timing error detector 605e and a variable oscillator 605g for newly generating the two times the frequency of the symbol clock according to the low pass component of the timing error information, and outputting to the A/D converter 601.

[0081][0080]   In such case of FIG. 6, the A/D converter 601 samples the analog passband signal from the two times the frequency of the symbol clock and converts into the digital passband signal. Therefore, the resampler is not required and burden on the hardware is reduced.

[0082][0081]   The output of the low pass filter 605f performing low pass filtering on the current timing error information detected from the timing error detector 605e is inputted to the variable oscillator 605g generating new two times the frequency of the symbol clock and the two times frequency (2fs) generated by using the low pass filtered timing error information from the variable oscillator 605g are inputted to the A/D converter 601. In this case, the roles of the squarers 605a and 605b, the adder 605c, the pre-filter 605d, the timing error detector 605e and the low pass filter 605f are the same as the same blocks of FIG. 5.

[0083][0082]   In other words, the digital passband I, Q signals ($I'''(t)$, $Q'''(t)$) inputted to the two squarers 605a and 605b is the same as the formula 7, the two squared signals ($\{I'''(t)\}^2, \{Q'''(t)\}^2$) outputted from the two squarers 605a and 605b are the same as the formula 8 and the output signal ($X'(t)$) from the additoner 605c is the same as the formula 9.

[0084][0083]   Therefore, there is an advantage of using the symbol clock recovery 605 that the symbol clock is recovered from the passband signal without being interfered by the carrier and the complexity of the hardware can be reduced resulted in removing of the resampler.

[0085][0084]   As mentioned above, there is an advantage that the symbol clock recovery is precisely and stably carried out from the signals not passed the carrier recovery 603, that is the mandatory process for the symbol clock recovery in the embodiment of FIG. 6. This describes that the symbol clock recovery 605 is able to operate and perform more stable symbol clock recovery regardless of the carrier signal component.

[0086][0085]   The symbol clock recovery in the embodiments of FIG. 3 and FIG. 6 employed two squarers and adders to the inputted signals for preventing reduced performance resulted from the incomplete performance of the carrier recovery. However, the squarer has a disadvantage that the size is getting larger when the hardware is employed and absolute value operators 706 and 707 can be employed instead of the squarers as described in FIG. 7. The symbol clock recovery not being interfered by the carrier modulator is realized to reduce the burden on the hardware and a carrier demodulator in FIG. 7.

[0087][0086]   The analog passband signal inputted to anthe A/D converter 701 is sampled as the output frequency of athe fixed oscillator 702 and converted into the digital signal. The output of the A/D converter 701 is passed through athe phase splitter 703, athe carrier recovery 704 and athe resampler 705, and then, inputted to the absolute value operators 706 and 707. The absolute value operatorsvalue caluculators 706 and 707 apply an absolute value to each of the digital baseband I, Q signals interpolated as two times the frequency of the symbol clock at the

24

resampler 705 and outputted, and outputs to ~~an~~the adder 708 to add. Influence of the carrier recovery 704 is totally removed from the output of the add~~it~~oner 708 as the same as the case the squarer~~a~~ is employed. The output of the adder 708 passes through ~~a~~the pre-filter 709, ~~a~~the ~~Gardner~~ timing error detector 710 and ~~a~~the low pass filter 711, and inputted to ~~an~~the NCO 712 to generate the two times the frequency of the symbol clock.

~~[0088]~~[0087]   As another embodiment of FIG. 7, the A/D converter 701 may receive the two symbol clock frequencies (2fs) from the variable oscillator instead of the fixed oscillator, and convert the analog passband signal into the digital passband signal using the two absolute value operators~~value-calculating-unit~~ instead of the two squarers. In this case, the resampler is not required.

~~[0089]~~[0088]   As the same in FIG. 7, if the symbol clock recovery is carried out from the output of the adder 708, the symbol clock recovery can be performed without being influenced by the carrier.

~~[0090]~~[0089]   Accordingly, as another embodiment of the present invention, the A/D converter converts the analog passband signal into the digital passband signal using the two times the frequency of the symbol clock. The symbol clock recovery receives, adds the digital passband real/imaginary signals outputted from the phase splitter and perform the symbol clock recovery.

[0091][0090]   In the embodiment of FIG. 3 and FIG. 6, the symbol clock recovery can be carried out nevertheless the two squarers are replaced with the two absolute value operatorsvalue calculating unit.

[0092][0091]   According to the digital TV receiver of the present invention, the symbol clock recovery is able to perform without being influenced by the remained carrier component after removing the remained carrier component using the two squarers and the adder. Therefore, the symbol clock recovery performs recovering symbol clock more stably even in the case the carrier recovery is not completely carried out.

[0093][0092]   Particularly, the present invention has an advantage that the symbol clock is recovered without being influenced by the carrier in case the symbol clock recovery is performed from the digital passband signal. Also, the burden on the hardware can be reduced using the two absolute value operatorscalculating unit instead of the two sqaurers.

[0094][0093]   As aforementioned, the symbol clock recovery performs without being influenced by the incomplete carrier component although the carrier recovery performs incomplete carrier recovery because of a heavy linear noise, i.e., ghost in a transmission channel. Therefore, the performance of the symbol clock recovery is enhanced, the burden on the hardware is reduced, and particularly, the carrier recovery let information on the rear of the channel equalizer used.

[0095][0094]   It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.